SiGe(C) MOSFET Technology

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• Issues in Scaled CMOS
• Bandstructure, Transport and Strain
• Enhanced Mobility Channels
  - Strained Si and SiGe(C)
• Multi-Gate and Novel MOSFETs
• Process Integration Challenges
### Table 47b  High-performance Logic Technology Requirements—Long-term

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2010</th>
<th>2012</th>
<th>2013</th>
<th>2015</th>
<th>2016</th>
<th>2018</th>
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<tr>
<td><strong>Technology Node</strong></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>DRAM ½ Pitch (nm)</td>
<td>hp45</td>
<td>45</td>
<td>35</td>
<td>32</td>
<td>25</td>
<td>22</td>
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<tr>
<td>MPU/ASIC Metal 1 (Δ1) ½ Pitch (nm)</td>
<td>34</td>
<td>42</td>
<td>38</td>
<td>30</td>
<td>27</td>
<td>21</td>
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<tr>
<td>MPU/ASIC ½ Pitch (nm)</td>
<td>45</td>
<td>35</td>
<td>32</td>
<td>25</td>
<td>22</td>
<td>18</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm)</td>
<td>25</td>
<td>20</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
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<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
<td>9</td>
<td>7</td>
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<tr>
<td>Physical gate length high-performance (HP) (nm) [1]</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
<td>9</td>
<td>7</td>
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<tr>
<td>EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.6</td>
<td>0.5</td>
<td>0.5</td>
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<tr>
<td>Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
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<tr>
<td>Equivalent electrical oxide thickness in inversion (nm) [4]</td>
<td>1.1</td>
<td>1.1</td>
<td>1.0</td>
<td>1.0</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>Nominal gate leakage current density limit (at 25°C) (A/cm²) [5]</td>
<td>1.9E+03</td>
<td>2.4E+03</td>
<td>7.7E+03</td>
<td>1.0E+04</td>
<td>1.5E+04</td>
<td>2.4E+04</td>
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<tr>
<td>Nominal power supply voltage (VDD) (V) [6]</td>
<td>1.0</td>
<td>0.9</td>
<td>0.9</td>
<td>0.8</td>
<td>0.8</td>
<td>0.7</td>
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<tr>
<td>Saturation threshold voltage (V) [7]</td>
<td>0.15</td>
<td>0.14</td>
<td>0.11</td>
<td>0.12</td>
<td>0.10</td>
<td>0.11</td>
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<tr>
<td>Nominal high-performance NMOS sub-threshold leakage current, I_DS leak (at 25°C) (mck/μm) [8]</td>
<td>0.1</td>
<td>0.1</td>
<td>0.3</td>
<td>0.3</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Nominal high-performance NMOS saturation drive current, I_Dsat (at VDD, at 25°C) (mck/μm) [9]</td>
<td>1900</td>
<td>1750</td>
<td>2050</td>
<td>2110</td>
<td>2400</td>
<td>2190</td>
</tr>
<tr>
<td>Required “mobility/transconductance improvement” factor [10]</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>Sub-threshold slope adjustment factor (Pull depletion/multiple-gate effects) (0–1) [11]</td>
<td>0.6</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
<td>1.3</td>
<td>1.3</td>
<td>1.3</td>
</tr>
<tr>
<td>Parasitic source/drain series resistance (R_SD) (Ohm-μm) [13]</td>
<td>135</td>
<td>116</td>
<td>107</td>
<td>88</td>
<td>79</td>
<td>60</td>
</tr>
<tr>
<td>Ideal NMOS device gate capacitance (F/μm) [14]</td>
<td>5.65E-16</td>
<td>4.39E-16</td>
<td>4.49E-16</td>
<td>3.45E-16</td>
<td>3.45E-16</td>
<td>2.69E-16</td>
</tr>
<tr>
<td>Parasitic fringe/overlap capacitance (F/μm) [15]</td>
<td>1.80E-16</td>
<td>1.50E-16</td>
<td>1.40E-16</td>
<td>1.20E-16</td>
<td>1.00E-16</td>
<td>8.00E-17</td>
</tr>
<tr>
<td>High-performance NMOS intrinsic delay, τ = C gate * VDD / I_Dsat (ps) [16]</td>
<td>0.39</td>
<td>0.30</td>
<td>0.26</td>
<td>0.18</td>
<td>0.15</td>
<td>0.11</td>
</tr>
<tr>
<td>Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]</td>
<td>3.06</td>
<td>4.05</td>
<td>4.64</td>
<td>6.80</td>
<td>8.08</td>
<td>10.77</td>
</tr>
<tr>
<td>Nominal logic gate delay (NAND gate) (ps) [18]</td>
<td>9.88</td>
<td>7.47</td>
<td>6.52</td>
<td>4.45</td>
<td>3.74</td>
<td>2.81</td>
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<tr>
<td>NMOSFET power-delay product (J/μm) [19]</td>
<td>7.45E-16</td>
<td>4.77E-16</td>
<td>4.77E-16</td>
<td>2.98E-16</td>
<td>2.85E-16</td>
<td>1.71E-16</td>
</tr>
<tr>
<td>NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]</td>
<td>1.10E-06</td>
<td>9.90E-07</td>
<td>2.97E-06</td>
<td>2.64E-06</td>
<td>4.40E-06</td>
<td>3.85E-06</td>
</tr>
</tbody>
</table>

Manufacturer solutions exist, and are being optimized
Manufacturer solutions are known
Interim solutions are known
Manufacturer solutions are NOT known
Experimental output characteristics of n-channel and p-channel MOSFETs with 0.1 micron channel lengths. The curves exhibit almost equal spacing, indicating a linear dependence of $I_D$ on $V_G$, rather than a quadratic dependence. We also see that $I_D$ is not constant but increases somewhat with $V_D$ in the saturation region. The p-channel devices have lower currents because hole mobilities are lower than electron mobilities.

For LONG channel

$$I_D = \frac{W}{L} \mu C_{0X} \left[ (V_G - V_T) V_D - \frac{1}{2} V_D^2 \right]$$

$$I_{DSAT} = \frac{W}{L} \mu C_{0X} \left[ (V_G - V_T) V_{DSAT} - \frac{1}{2} V_{DSAT}^2 \right]$$

where $[V_{DSAT} = (V_G - V_T)]$

For SHORT channel,

$$I_D \approx WC_{OX} (V_G - V_T) V_{sat}$$
For short “quasi-ballistic” MOSFETs, current is limited by source-to-channel injection of thermal carriers. Since, here the longitudinal field is low, **this injection is limited by low field mobility.** (Natori and Lundstrom)
Compressive Strain in $\text{Si}_{1-x}\text{Ge}_x$

- $\text{Si}_{1-x}\text{Ge}_x$ Bulk Properties.
  - 0 to 100% Ge possible
  - Lattice constant and bandgap given by Vegard’s Law:
    \[ a_{\text{SiGe}}(x) = a_{\text{Si}}(1-x) + a_{\text{Ge}}(x) \]
- $\text{Si}_{1-x}\text{Ge}_x$ on Si
  - Up to 4.2% lattice mismatch
  - Strained epitaxial layers
  - Tetragonal distortion breaks degeneracy in the bandstructure.
Bandstructure effective mass, $m^*$, is inversely related to curvature of bands, and depends on crystal orientation. Density of states $m^*$ is related to geometric mean of bandstructure $m^*$. Must count number of “equivalent” valleys. Conductivity $m^*$ is harmonic mean of bandstructure $m^*$.

**Effective mass**

$$m^* = \frac{\hbar^2}{\left( \frac{d^2 E}{dk^2} \right)}$$

$$\mu = \frac{e\langle \tau \rangle}{m^*}$$

$$g_c(E) = 4\pi \left( \frac{m_{de}^*}{\hbar^2} \right)^2 (E-E_c)^\frac{1}{2}$$

$$m^* = \left( m_1^* m_2^* m_3^* \right)^\frac{1}{3}$$

$$m^* = 3 \left( \frac{1}{m_1^*} + \frac{1}{m_2^*} + \frac{1}{m_3^*} \right)^{-1}$$
Si-based Strained Materials

CB

VB

Bulk Si

CS-SiGe

HH

LH

CS-SiGe

HH

LH

TS-Si

Relaxed SiGe

CB

VB

TS-Si

Relaxed SiGe
Calculated Electron and Hole Mobility of Strained SiGe
Hole mobility with/without alloy scattering in plane and out-of-plane

Electron mobility with/without alloy scattering in plane and out-of-plane

Fischetti and S.E. Laux, J. Appl. Phys. 80 (4), 1996
Monte Carlo calculations of minority hole mobilities in Si$_{1-x}$Ge$_x$ for four doping levels (in cm$^{-3}$) at 300 K: dot-dashed line is the vertical mobility of strained Si$_{1-x}$Ge$_x$, solid line is the mobility of unstrained Si$_{1-x}$Ge$_x$, dashed line is the planar mobility of strained Si$_{1-x}$Ge$_x$.

Ultra High Vacuum Chemical Vapor Deposition

- Base pressure: ~$10^{-10}$ Torr
- Cold wall, load locked system
- Low deposition pressures
  - 1 to 10 mTorr
- ~500° C growth temperature
- Gases
  - $\text{Si}_2\text{H}_6$, $\text{GeH}_4$, $\text{CH}_3\text{SiH}_3$
  - $\text{B}_2\text{H}_6$, $\text{PH}_3$

- Can use hot wall UHVCVD or RTPCVD
Enhanced-Mobility Strained-Si n-MOSFETs

Surface Channel

Si$_{1-y}$Ge$_y$ Graded buffer

$y = 0.05$ to $x$

HIGH MOBILITY DEVICES - STRAINED SI CHANNELS:

Welser, et al. IEDM 1992

M. Jurczak et al., ESSDERC 1999
Strained Si-on-SiGe Buffer

Mobility Enhancements in Surface-channel Strained-Si MOSFETs

Conduction band

Bulk Si

Strained Si

\( \Delta E_s \sim 67 \cdot \text{meV/10\% Ge} \)

Valence band

\( \Delta E_s \sim 40 \text{ meV/10\% Ge} \)

NMOS

PMOS

Substrate Ge fraction, \( x \)

Substrate Ge Content (%)

Mobility enhancement ratio

Mobility Enhancement Factor

Calculated for strained Si MOS inversion layer


Calculation by Oberhuber et al.

Rim, et al.

Currie and Leitz, et al.
Inversion Layer Mobility

Strained Si mobility enhancement may be due to reduced surface roughness, rather than bandstructure (Fischetti)

Matthiessen’s rule:

\[
\frac{1}{\mu} = \frac{1}{\mu_{\text{Coulomb}}} + \frac{1}{\mu_{\text{phonon}}} + \frac{1}{\mu_{\text{surface-roughness}}} + \frac{1}{\mu_{\text{universal}}}
\]

- Doping dependent mobility model incorporated into existing mobility model in MEDICI device simulator.

\[(Lombardi, et al.)\]

\[
\mu_{\text{coulomb}} = An^\alpha N_a^{-\beta} \quad \mu_{\text{sr}} = \frac{\delta}{E_\perp} \quad \mu_{\text{phonon}} = \frac{a}{E_\perp} + \frac{\beta N_a^{0.0284}}{T(E_\perp)^{1/3}}
\]
Strained Si NMOSFET Monte Carlo Simulations

- MIT well-tempered device structure: http://www-mtl.mit.edu/Well/device50/topology50.html
- 1-D Schrödinger equation for quantum correction
- As suggested by Fischetti et. al., J. Appl. Phys., 92 (12), 2002), surface roughness reduction may play a role in mobility increase in strained-Si devices.
Current enhancement in Strained Si NMOSFET
Strained Si $\rho$-MOSFETs

- $\mu_{\text{eff}}$ enhancement decreases with gate overdrive* for holes
  - No $p$-channel enhancement at $E_{\text{eff}} = 1 \text{ MV/cm}^{**}$ for $x = 0.28$
  - Physical mechanism poorly understood

**Performance benefits of $\varepsilon$-Si primarily from $n$-MOSFET**
Mobility enhancement in tensile and compressively strained Si
# Mobility with Strain (Courtesy: Yu)

<table>
<thead>
<tr>
<th></th>
<th>Compressive</th>
<th>Un-strained</th>
<th>Tensile</th>
</tr>
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<tbody>
<tr>
<td>Si</td>
<td>e: degraded</td>
<td>-</td>
<td>e: enhanced</td>
</tr>
<tr>
<td></td>
<td>p: enhanced</td>
<td></td>
<td>p: degraded (stress&lt;1MPa)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>p: enhanced (stress&gt;1MPa)</td>
</tr>
<tr>
<td>SiGe</td>
<td>e: degraded</td>
<td>e: degraded</td>
<td>e: enhanced</td>
</tr>
<tr>
<td></td>
<td>p: enhanced</td>
<td>(Ge&lt;0.8)</td>
<td>(Ge&lt;0.2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>e: enhanced</td>
<td>e: degraded (Ge&gt;0.2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Ge&gt;0.8)</td>
<td>p: enhanced (Ge&lt;0.3)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>p: degraded</td>
<td>p: degraded (Ge&gt;0.3)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Ge&lt;0.7)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>p: enhanced</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Ge&gt;0.7)</td>
<td></td>
</tr>
</tbody>
</table>
SiGe strain- and band-engineered heterostructures

- Relaxed $\text{Si}_{1-x}\text{Ge}_x$ virtual substrates allow
  - Si-rich alloys in biaxial tension ($a_\parallel/a_0 > 1$)
    - Type-II band offset $\rightarrow$ Two-dimensional electron gas
    - Barrier for holes
  - Ge-rich alloys in biaxial compression ($a_\parallel/a_0 < 1$)
    - Type-I band offset $\rightarrow$ Two-dimensional hole gas
    - Cannot confine electrons
Dual-channel heterostructures

- Cannot confine $\psi$ in one channel or another
  - Different from traditional buried-channel device
- $\varepsilon$-$\text{Si}_{1-y}\text{Ge}_y$ layer beneath $\varepsilon$-Si boosts $\mu_{\text{eff}}$ even at large $N_{\text{inv}}$, high $E_{\text{eff}}$
- $\varepsilon$-Si is more than just a “cap”
  - Enhanced hole mobility*, different from pseudomorphic SiGe devices

$$x = 0.2 \quad \text{or} \quad x = 0.3$$
$$y = 0.5 \quad \text{or} \quad y = 0.6$$
Figure 1 Schematic view of 3D process-induced strain components.

TABLE I Impact of 3D Strain Effects on CMOS Performance.
*Strain change = increased tensile or decreased compressive strain

<table>
<thead>
<tr>
<th>Direction of Strain Change*</th>
<th>CMOS Performance Impact</th>
<th>CMOS Performance Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>X</td>
<td>Improve</td>
<td>Degrade</td>
</tr>
<tr>
<td>Y</td>
<td>Improve</td>
<td>Improve</td>
</tr>
<tr>
<td>Z</td>
<td>Degrade</td>
<td>Improve</td>
</tr>
</tbody>
</table>

3D Strain Sensitivity of CMOS Current Drive

Figure 3 $I_{on}$ vs. $I_{off}$ characteristics at 1V operating voltage. Up to 15% improvement is achieved in NMOS and PMOS with cap-layer-, STI- and silicide-strained Si.

Ge, et. al, IEDM 2003
Sanuki, et. al. IEDM 2003

Diagram showing the effect of stress on electron and hole mobility in a strained Si layer. The diagram compares the effects of large and small L_SD on the mobility modulation by STI stress.
Electronic Properties of Strained Si$_{1-x}$Ge$_x$

Type-I (Compressive)
SiGe MOSFET Structure

- Typical MOS structure
  - $\text{Si}_{1-x}\text{Ge}_x$ channel with Si cap leads to buried channel, and lower gate capacitance

- Si cap
  - Used for oxidation
  - Also acts as a parasitic channel, leading to gate operating “window”

Output, sub-threshold, and mobility-field characteristics of 70nm Si$_{0.9}$Ge$_{0.1}$-SiO$_2$ buried channel PHFET.

Subthreshold and mobility-field characteristics for 180nm Si$_{0.8}$Ge$_{0.2}$-HfO$_2$ PHFETs and control Si PMOSFET.

**Recovery of mobility degradation for high-k gate dielectrics with enhanced-mobility channels:** (Onsongo,.., Banerjee)

Addition of C to Si and Si$_{1-x}$Ge$_x$

- Carbon has a smaller lattice constant
  - Strain compensation of SiGe (~8:1)
  - Tensile strained Si-C on Si
- Low solubility in Si
  - Need low temperature growth to incorporate C due to low solubility (5x10$^{17}$ cm$^{-3}$)
  - Growth window for alloy growth
- Carbon $\Delta E_v = 21-26$ meV/%C in SiGeC (Lanzerotti, EDL, 1996)
  - Ge $\Delta E_v = 25$ meV/3% Ge
- Carbon $\Delta E_c = 75-90$ meV/%C for SiC
  - (Faschinger, APL, 1995)


Carbon Strain Compensation

\[ \text{Si}_{0.585}\text{Ge}_{0.4}\text{C}_{0.015} \text{ shows 55\% drive current enhancement over bulk Si and 42\% enhancement over Si}_{0.6}\text{Ge}_{0.4} } \]

W/L = 10/0.5 um; tox = 6 nm

Electronic Properties of Strained Si$_{1-x}$Ge$_x$

- Strain splits the six fold degeneracy of conduction band valleys.
- The four-fold in-plane valleys are lowered, leading to less f-type scattering.
- Carriers have a lower out-of-plane and higher in-plane mass.
- Electron mobility dependent on directions: increase in $\perp$, decrease in $||$
- To enhance electron mobility for the planar NMOSFETs, tensile strained Si has to be used.

- Hole mobility increases with Ge fraction.
  - Valence band splitting with strain results in reduced scattering.
  - Reduction of effective hole mass with strain due to VB warpage
  - Increase in both $\perp$ and $||$ mobilities

Chen XD, Banerjee SK, Hole and electron mobility enhancement in strained SiGe vertical MOSFETs, IEEE T ELECTRON DEV 48 (9): 1975-1980 SEP 2001
Hole mobility in Strained SiGe

- In tensile SiGe, hole mobility decreases as Ge% increase.
- Enhanced below 30% Ge.

In compressive SiGe, hole mobility increases as Ge% increase.
Mobility in Relaxed SiGe

- Mobility degraded for most of Ge% 
- Only become higher at >80% Ge 
- Alloy scattering is blamed for degradation

Vertical Si, relaxed and strained Si$_{1-x}$Ge$_x$ PHFETs showing enhancement of drive current over Si MOSFETs only in the presence of strain. 
NHFETs also enhanced!

Jayanaran & Banerjee, EMC 2004
Ge MOSFETs

<table>
<thead>
<tr>
<th></th>
<th>Ge</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\mu_n$ (cm$^2$/Vs)</td>
<td>3900</td>
<td>1500</td>
</tr>
<tr>
<td>$\mu_p$ (cm$^2$/Vs)</td>
<td>1900</td>
<td>450</td>
</tr>
<tr>
<td>Eg (eV)</td>
<td>0.66</td>
<td>1.12</td>
</tr>
</tbody>
</table>

- Bulk Ge has higher electron (2.5x) and hole (4x) mobility than Si, and can potentially lead to faster MOSFETs and more balanced N vs. PMOSFETs.
- Germanium bulk substrates brittle, lower thermal conductivity (0.6W/cm-K vs. 1.5 for Si)
- Smaller Ge bandgap than Si broadens absorption spectrum; optoelectronic integration on CMOS?
- Native oxide on Ge surface is not stable; GeO$_2$ water soluble, GeO volatile at low T. Deposited high-k gate dielectrics promising
- Performance much worse than expected, especially for NMOSFETs, probably because of poor interface between Ge and high-k gate dielectric, as well as poor dopant activation and interface between metal- source/drain
- Higher junction leakage in Ge, especially at high T
- Higher dielectric constant in Ge leads to worse electrostatics (DIBL, SS)
UHVCVD Ge-on-Si NMOS w/o SiGe buffer with PVD HfO2 and TaN gate

- Capacitance (uF/cm²) vs. VG (V)
  - EOT = 1.1 nm
  - L = 10 um, W = 100 um

- IS (A/um) vs. VG (V)
  - L = 2 um, W = 5 um
  - SS = 170 mV/dec
  - Vt ~ 0.3 V

- Ig (A/cm²) vs. VG (V)
  - L = 10 um, W = 100 um
  - EOT = 1.1 nm

Donnelly, ., Banerjee, SRC 2004
Effect of strain in Ge layer

- Higher strain in the Ge layer favors high $\mu_{\text{eff}}^*$
  - $x \leq 0.7$
    - reasonable agreement with theoretical calculations**
  - $x \geq 0.8$
    - rampant defect nucleation in Si cap, $\mu_{\text{eff}}$ depressed

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3-D Transistor Structures

IBM '97

Berkeley '99

Lucent '99

Mark Bohr, ECS Meeting PV 2001-2, Spring, 2001
Strained-Si PMOSFET on SiGe-on-Insulator

T. Mizuno et al., IEDM, 934-936 (1999)
SSOI with thin SiGe buffers w/o misfits using BPSG compliant substrates

Rim, et. al. & Sturm et. al. (IEDM, 2003)
High mobility heterojunction transistor (HMHJT)

- A Si/SiGe/Si quantum well is used to increase the drive current.

- The bulk punchthrough, DIBL and floating body effect are still suppressed due to heterojunction in the deep source/drain region.

Energy Band Diagram and Hole Concentration of HMHJT in the Channel

- $E_v$ (eV)
- Hole Concentration ($cm^{-3}$)

$V_{DS} = V_{GS} = -2V$

1 nm from the surface

Source Channel Drain
Subthreshold and Output Characteristics for HMHJT

![Graphs showing subthreshold and output characteristics for HMHJT](image)

**Graph 1:**
- $I_D$ vs. $V_{GS}$
- $V_{DS} = -0.1, -0.6, -1.1, -1.6$ V
- Lines for Si control and HMHJT

**Graph 2:**
- $I_D$ vs. $V_{DS}$
- Lines for Si control device and HMHJT
- $V_{GT} = 0, -0.5, -1, -1.5, -2$ V
Process Issues

- Strain relaxation
  - Require low process temperature and thermal budget

- Leakage concerns
  - Defect/ dislocation density in active device layers
  - Smaller bandgap

- Self-heating
  - Much poorer thermal conductivity of SiGe layers
  - Thick gradual SiGe buffer layer

- STI edge leakage can be increased by SiGe buffer.

- B diffusion enhanced by tensile strain; compressive retards it. Ge retards B and enhances As/P diffusion in SiGe buffer.

- Need higher doping in channel due to reduced bandgap- negates some advantages of strain
Defects in Strained Si

(a) Source: MIT/Fitzgerald Group

Strain: 1% mismatch ~ 1GPa, Si-Ge: 4%, Tensile in Si

Critical Thickness

Defect Density

Source: Chris Leitz’s thesis

$h_c$ (Å)

% Ge

1E+8

1E+7

1E+6

1E+5

% Ge
Takagi, et. al, IEDM 2003

\[ \Delta E_c \Rightarrow \Phi_B \uparrow \Rightarrow I_{\text{tunnel}} \downarrow \]

\[ J_g = I_{\text{tunnel}} \]

\[ \Delta E_c = 0.57 x_{\text{eff}} \text{ [eV]} \]

\[ \Delta E_c \Rightarrow V_{\text{th}} \downarrow \text{ (Ge content: } x_{\text{eff}} \text{)} \]

\[ \text{without strain} \rightarrow \text{tensile strain} \]
Device Metrics

- **Speed**
  - \( \tau = \frac{C_{\text{load}} V_{\text{DD}}}{I_d} \)

- **Power**
  - \( P = f \ C_{\text{load}} V_{\text{DD}}^2 \)

- **Saturation current**
  - \( I_{\text{DSAT}} = \frac{(W/2L) (k_r k_o A) (T_{\text{EOT,INV}})^{-1} \mu (V_G-V_T)^2}{(V_G-V_T)} \)
    - Consider \( V_G \Rightarrow V_{\text{DD}} \)

- **Transconductance**
  - \( g_m = \frac{(W/L) (k_r k_o A) (T_{\text{EOT,INV}})^{-1} \mu V_{\text{DSAT}}}{(V_G-V_T)} \)

- **Off-state power**
  - Subthreshold swing and source/drain junction leakage